AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for manufacturing a semiconductor device comprising:

forming plural interconnection lines, each comprising an interconnection layer, a capping layer, the capping layer defining a contact resistance, and an etching stopper, on a semiconductor substrate;

forming an interlayer insulating layer overlying the plural interconnection lines, wherein the thickness of a portion of the interlayer insulating layer on one of the etching stoppers is different from the thickness of a portion of the interlayer insulating layer on the others;

etching the interlayer insulating layer to form first contact holes therein;

stopping etching when a top surface of each etching stopper is exposed;

removing a portion of each etching stopper exposed by the first contact holes by performing a dry etching method using an etchant having a low etching selectivity between the etching stopper and the capping layer, thereby forming second contact holes, and leaving the capping layers of the plural interconnection lines at substantially the same thickness such that the contact resistances of the plural interconnection lines are substantially uniform; and

forming a conductive layer within the second contact holes,

wherein the interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing a first material layer for interconnection, a second material layer for capping, and a third material layer for stopping etching, patterning the third material layer, and then patterning the second and first material layers, using the patterned third material layer.

2. (Previously presented) The method for manufacturing a semiconductor device of claim 1 further comprising forming third contact holes by slightly etching a portion of the capping layer exposed by the second contact holes before forming the conductive layer, and wherein the conductive layer is formed within the second contact holes and the third contact holes.

3. (Original) The method for manufacturing a semiconductor device of claim 2, wherein the conductive layer is formed only in the second and third contact holes.

4. (Original) The method for manufacturing a semiconductor device of claim 2, wherein the conductive layer is an upper interconnection layer filling the second and third contact holes and covering the top surface of the interlayer insulating layer.

5. (Currently amended) The method for manufacturing a semiconductor device of claim 2 wherein the ~~second and~~ third contact holes are formed by performing a dry etching method using an etchant having a low etching selectivity between the etching stopper and the capping layer.

6. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the etching stopper is formed of an inorganic anti-reflecting layer (ARL) or an organic anti-reflecting coating (ARC).

7. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the interconnection layer is a metal layer containing aluminum.

8. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the capping layer is formed of TiN, Ti/TiN or TaN.

9. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the interlayer insulating layer is formed of one selected from the group consisting of a silicon oxide layer, a silicon nitride layer, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG), tetraethylorthosilicate (TEOS), plasma enhanced TEOS (PE-TEOS), and undoped silicate glass (USG).

10. (Cancelled)

11. (Previously presented) The method for manufacturing a semiconductor device of claim 1, wherein the conductive layer is formed only in the second contact holes.

12. (Previously presented) The method for manufacturing a semiconductor device of claim 1, wherein the conductive layer is an upper interconnection layer filling the second contact holes and covering the top surface of the interlayer insulating layer.

13. (Previously presented) The method for manufacturing a semiconductor device of claim 1, wherein the first contact holes are formed by using a dry etching method.

14. (Withdrawn) A semiconductor device comprising:

a semiconductor substrate;

a interconnection layer formed on the semiconductor substrate;

a capping layer formed on the interconnection layer;

an etching stopper formed on the capping layer;

an interlaying insulating layer having a contact hole overlying the interconnection layer, the contact hole formed through the etching stopper to substantially expose a portion of the capping layer; and

a conductive material layer disposed within the contact hole.

15. (Withdrawn) The semiconductor device of claim 14, wherein the etching stopper is adjacent to sidewalls of the contact hole.

16. (Withdrawn) The semiconductor device of claim 14, the etching stopper is formed of an inorganic anti-reflecting layer (ARL) or an organic anti-reflecting coating (ARC).

17. (Withdrawn) The semiconductor device of claim 14, wherein the interconnection layer is a metal layer containing aluminum.

18. (Withdrawn) The semiconductor device of claim 14, wherein the capping layer is formed of a material selected from the group consisting of TiN, Ti/TiN, and TaN.

19. (Withdrawn) The semiconductor device of claim 14, wherein the conductive layer is formed only in the contact hole.

20. (Withdrawn) The semiconductor device of claim 14, wherein the conductive layer is an upper interconnection layer filling the contact hole and covering the top surface of the interlayer insulating layer.

21. (Previously presented) The method for manufacturing a semiconductor device of claim 1, wherein the capping layers are etched to form a uniform thickness among the second contact holes.

22. (Previously presented) The method for manufacturing a semiconductor device of claim 1, wherein the second contact holes expose a top surface of the capping layers.

23-25 (Cancelled)

26. (Previously presented) A method for manufacturing a semiconductor device comprising:

forming plural interconnection lines, each including an interconnection layer, a capping layer and an etching stopper, on a semiconductor substrate;

forming an interlayer insulating layer overlying the plural interconnection lines, wherein the thickness of a portion of the interlayer insulating layer on one of the etching stoppers is different from the thickness of a portion of the interlayer insulating layer on the others;

first etching the interlayer insulating layer to form first contact holes therein using a first etchant having a high etching selectivity between the etching stopper and the interlayer insulating layer;

second etching a portion of each etching stopper exposed by the first contact holes, using a second etchant having a low etching selectivity between the etching stopper and the capping layer, thereby forming second contact holes; and

forming a conductive layer within the second contact holes,

wherein the interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing a first material layer for interconnection, a second material layer for capping, and a third material layer for stopping etching, patterning the third material layer, and then patterning the second and first material layers using the patterned third material layer.

27. (Previously presented) The method of claim 26, further comprising: stopping etching when a top surface of each etching stopper is exposed.